

International application No
PCT/EP2005/054928

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|-----------|---|-----------------------|
| X | <p>HAMMOUDA S ET AL: "A fully automated approach for analog circuit reuse" SYSTEM-ON-CHIP FOR REAL-TIME APPLICATIONS, 2004.PROCEEDINGS. 4TH IEEE INTERNATIONAL WORKSHOP ON BANFF, AB, CANADA 19-21 JULY 2004, PISCATAWAY, NJ, USA,IEEE, 19 July 2004 (2004-07-19), pages 237-240, XP010714038 ISBN: 0-7695-2182-7 the whole document</p> <p style="text-align: center;">----- -/--</p> | 1-18 |

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

26 April 2006

Date of mailing of the international search report

08/05/2006

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INTERNATIONAL SEARCH REPORT

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| C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT | | |
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| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
| X | HAMMOUDA S ET AL: "Analog IP migration using design knowledge extraction" CUSTOM INTEGRATED CIRCUITS CONFERENCE, 2004. PROCEEDINGS OF THE IEEE 2004 ORLANDO, FL, USA OCT. 3-6, 2004, PISCATAWAY, NJ, USA, IEEE, 3 October 2004 (2004-10-03), pages 333-336, XP010742307 ISBN: 0-7803-8495-4 the whole document | 1-18 |
| X | XU JINGNAN ET AL: "IC design automation from circuit level optimization to retargetable layout" ELECTRONICS, CIRCUITS AND SYSTEMS, 2001. ICECS 2001. THE 8TH IEEE INTERNATIONAL CONFERENCE ON 2-5 SEPTEMBER 2001, PISCATAWAY, NJ, USA, IEEE, vol. 1, 2 September 2001 (2001-09-02), pages 95-98, XP010562944 ISBN: 0-7803-7057-0 the whole document | 1-18 |
| X | FUNABA S ET AL: "A fast and accurate method of redesigning analog subcircuits for technology scaling" DESIGN AUTOMATION CONFERENCE 1998. PROCEEDINGS OF THE ASP-DAC '98. ASIA AND SOUTH PACIFIC YOKOHAMA, JAPAN 10-13 FEB. 1998, NEW YORK, NY, USA, IEEE, US, 10 February 1998 (1998-02-10), pages 489-494, XP010275914 ISBN: 0-7803-4425-1 the whole document | 1-18 |
| X | PHELPS R ET AL: "A case study of synthesis for industrial-scale analog IP: redesign of the equalizer/filter frontend for an ADSL codec" PROCEEDINGS OF THE 37TH. ANNUAL DESIGN AUTOMATION CONFERENCE. (DAC). LOS ANGELES, CA, JUNE 5-9, 2000, PROCEEDINGS OF THE DESIGN AUTOMATION CONFERENCE, NEW YORK, NY : IEEE, US, 5 June 2000 (2000-06-05), pages 1-6, XP002186438 ISBN: 0-7803-6315-9 the whole document | 1-18 |
| X | US 2005/028113 A1 (LIN YIQUN ET AL) 3 February 2005 (2005-02-03) paragraph [0001] paragraph [0005] - paragraph [0008] paragraph [0024] - paragraph [0029] paragraph [0035] - paragraph [0036] | 1-18 |

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2005/054928

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---------------------|----------------------------|---------------------|
| US 2005028113 | A1 | 03-02-2005 | NONE |